WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

first and second CMOS (complementary metal oxide semiconductor) inverter circuits each having a latch structure;

a control transistor which is connected between a storage node of the first CMOS inverter circuit and a bit line and whose gate is connected to a word line; and

a selection circuit to apply one of a first voltage and a second voltage different from the first voltage to a power supply node of at least the second CMOS inverter circuit,

wherein the selection circuit applies the second voltage to the power supply node of the second CMOS inverter circuit at least in "1" data write mode.

2. The semiconductor memory device according to claim 1, wherein the first voltage is a voltage VDD and the second voltage is a voltage VDD-ΔV (ΔV > 0).

3. The semiconductor memory device according to claim 2, wherein the voltage VDD-ΔV is set at 95% to 70% of the voltage VDD.

4. The semiconductor memory device according to claim 1, wherein the selection circuit is a power supply selection switch to switch between a first power supply which supplies the first voltage and a second power supply which supplies the second voltage, and

the power supply selection switch is controlled in accordance with rise timing of the word line.

5. The semiconductor memory device according to claim 1, wherein the selection circuit includes a capacitor inserted in a VDD power line, a switching transistor connected in series to the capacitor, and a logic circuit which turns on and off the switching transistor.

6. The semiconductor memory device according to claim 5, wherein the logic circuit includes a NAND circuit which performs a NAND operation for an AND output of a word line selection signal and a write enable signal and a bit line selection signal, and the NAND circuit turns on the switching transistor only in the "1" data write mode.

7. The semiconductor memory device according to claim 5, wherein the logic circuit includes a NAND circuit which performs a NAND operation for a write enable signal and a bit line selection signal, and the NAND circuit turns on the switching transistor in "1" data write mode and "0" data write mode.

8. The semiconductor memory device according to claim 1, wherein the selection circuit applies the second voltage to a power supply node of the first CMOS inverter circuit at least in the "1" data write mode.

9. The semiconductor memory device according to claim 1, wherein the first voltage is a voltage VSS and

the second voltage is a voltage VSS+ΔV (ΔV > 0).

10. The semiconductor memory device according to claim 9, wherein the voltage VSS+ΔV is set at 105% to 130% of the voltage VSS.

11. A semiconductor memory device having a memory structure in which a plurality of 5-transistor cells each including first and second CMOS (complementary metal oxide semiconductor) inverter circuits each having a latch structure and a control transistor which is connected between a storage node of the first CMOS inverter circuit and a bit line and whose gate is connected to a word line are connected in parallel to a plurality of bit lines and a plurality of word lines, the semiconductor memory device comprising:

at least one VDD power line connected to a source terminal of a P-type MOS transistor of at least the second CMOS inverter circuit of each of the 5-transistor cells connected to the bit lines; and

at least one selection circuit which applies a second voltage VDD-ΔV, which is lower than a first voltage VDD, to the source terminal of the P-type MOS transistor of the second CMOS inverter circuit of the 5-transistor cells through said at least one VDD power line at least in "1" data write mode.

12. The semiconductor memory device according to claim 11, wherein the second voltage VDD-ΔV is set at 95% to 70% of the first voltage VDD.

13. The semiconductor memory device according to claim 11, wherein said at least one VDD power line is connected to a source terminal of a P-type MOS transistor of the first CMOS inverter circuit of each of the 5-transistor cells connected to the bit lines, and said at least one selection circuit applies the second voltage VDD-ΔV to source terminals of P-type MOS transistors of the first and second CMOS inverter circuits of the 5-transistor cells through said at least one VDD power line at least in the "1" data write mode.

14. A semiconductor memory device having a memory structure in which a plurality of 5-transistor cells each including first and second CMOS (complementary metal oxide semiconductor) inverter circuits each having a latch structure and a control transistor which is connected between a storage node of the first CMOS inverter circuit and a bit line and whose gate is connected to a word line are connected in parallel to a plurality of bit lines and a plurality of word lines, the semiconductor memory device comprising:

at least one VSS power line connected to a source terminal of an N-type MOS transistor of at least the second CMOS inverter circuit of each of the 5-transistor cells connected to the bit lines; and

at least one selection circuit which applies a second voltage VSS+ΔV, which is higher than a first

voltage VSS, to the source terminal of the N-type MOS transistor of the second CMOS inverter circuit of the 5-transistor cells through said at least one VSS power line at least in "1" data write mode.

15. The semiconductor memory device according to claim 14, wherein the second voltage VSS+ΔV is set at 105% to 130% of the first voltage VSS.

16. The semiconductor memory device according to claim 14, wherein said at least one VSS power line is connected to a source terminal of an N-type MOS transistor of the first CMOS inverter circuit of each of the 5-transistor cells connected to the bit lines, and said at least one selection circuit applies the second voltage VSS+ΔV to source terminals of N-type MOS transistors of the first and second CMOS inverter circuits of the 5-transistor cells through said at least one VSS power line at least in the "1" data write mode.